ABSTRACT OF THE DISCLOSURE

A signal processing circuit is provided which can perform high-speed image rotation, reflection, and the like, by such a configuration that an image input apparatus, e.g., a digital still camera, has a coprocessor connected to a CPU; the coprocessor has register groups (RG1 to RG4) which are electrically connected one another, each register group having registers (R1 to R4) of 32 bits length; and the registers (R1 to R4) store a one-byte image data in the zero-th to third bytes, respectively. When an image data read from the CPU to the register group (RG3) is transferred to the register group (RG1) through the register group (RG2), the image can be rotated 90 degrees counterclockwise. Also, other processing such as a clockwise 90 degrees rotation, symmetrical reflection in horizontal direction, etc. can be conducted at a high speed, without converting the data length of an image data.